In the Claims:

Please amend claims 1-3, 15, 16, 21 and 22. Please cancel claims 17 and 18. Please add new claims 23-30.

The claims are as follows:

1. (Currently Amended) A method, comprising in the order recited:

(a) placing a DDR DRAM having a test mode and an operational mode in test mode, said DDR RAM comprising an array of storage cells arranged in rows and columns, storage cells each row addressable by a respective wordline of a set of wordlines and each storage cells in each column addressable by a respective bitline of a set of bitlines;

(b) issuing a bank activate command on an occurrence of a rising edge of a first clock signal of a pair of adjacent clock signals of a test clock to select and bring up a wordline selected from said set of wordlines for write of said ~~DDR DRAM~~ wordline selected for write;

(c) ~~writing~~ issuing a write with auto-precharge [,] command on an occurrence of a rising edge of a second clock signal of said pair of adjacent clock signals to write a test pattern to storage cells ~~of said DDR DRAM~~ corresponding to said wordline selected for write;

(d) repeating steps (b) and (c) until all wordlines of said set of wordlines ~~for write~~ have been selected and written;

(e) issuing a bank activate command on an occurrence of a rising edge of a first clock signal of a subsequent pair of adjacent clock signals to select and bring up a wordline selected from said set of wordlines for read of said ~~DDR DRAM~~ wordline selected for read;

(f) ~~reading~~ issuing a read with auto-precharge [,] command on an occurrence of a rising edge of a second clock signal of said subsequent pair of adjacent clock signals to read the stored

test pattern from storage cells ~~of said DDR DRAM~~ corresponding to said wordline selected for read; and

(g) repeating steps (e) and (f) until all wordlines of said set of wordlines ~~for read~~ have been selected and read.

2. (Currently Amended) The method of claim 1, wherein ~~each of steps (b), (c), (e) and (f) each take~~ a read column address select latency of said DDR DRAM is one clock cycle of said test clock.

3. (Currently Amended) The method of claim 1, further including before step (a), the step of heating said DDR DRAM to ~~a predetermined~~ an elevated temperature greater than room temperature.

4. (Original) The method of claim 1, wherein said DDR DRAM is operating at a clock frequency below about one MHz in said test mode.

5. (Original) The method of claim 1, wherein an amount of elapsed time between writing to and reading from a storage cell accessible by a particular wordline and bitline combination does not exceed a retention time specification of said storage cell.

6. (Original) The method of claim 1, wherein peripheral logic circuits of said DDR DRAM are adapted to execute a write burst enable and a column address command one clock cycle earlier in test mode than in operational mode, adapted to execute an auto-precharge enable one-half clock

cycle earlier in test mode than in operational mode, and having a column address latency of one clock cycle in test mode and two or three clock cycles in operational mode.

7. (Original) The method of claim 1, wherein:

said DDR DRAM is adapted to initiate, in a timed auto-precharge mode of said test mode, a precharge immediately after a falling edge of a clock cycle; and

said DDR DRAM is adapted to, in a non-timed auto-precharge mode of said test mode, to start an auto-precharge asynchronously after the falling edge of a clock cycle and after a timer allows enough time for a write-back to said DDR DRAM.

8. (Withdrawn) A DDR DRAM having a low frequency and a high frequency operating mode, comprising:

a multiplicity of storage cells arranged in an array, each storage cell accessible by a wordline and a bitline; and

wherein peripheral logic circuits of said DDR DRAM are adapted to execute a write burst enable and a column address command one clock cycle earlier in low frequency operating mode than in high frequency operating mode, adapted to execute an auto-precharge enable one-half clock cycle earlier in low frequency operating mode than in high frequency operating mode, and having a column address latency of one clock cycle in test mode and two or three clock cycles in operational mode.

9. (Withdrawn) The DDR DRAM of claim 8, wherein said DDR DRAM is operating at a clock frequency below about 33 MHz in low frequency mode and at a clock frequency above about 33 MHz in high frequency mode.

10. (Withdrawn) The DDR DRAM of claim 8, wherein writing to a particular storage cell takes two clock cycles in low frequency operational mode and five clock cycles in high frequency operational mode.

11. (Withdrawn) The DDR DRAM of claim 10, wherein said DDR DRAM, during writing to said particular storage cell in low frequency mode is responsive to a bank activate command during a first clock cycle and responsive to a write with auto-precharge command during a second clock cycle.

12. (Withdrawn) The DDR DRAM of claim 10, wherein said DDR DRAM, during reading from said particular storage cell in low frequency mode is responsive to a bank activate command during a first clock cycle, responsive to a write command during a second clock cycle and responsive to a precharge command during a fifth clock cycle.

13. (Withdrawn) The DDR DRAM of claim 8, wherein reading from a particular storage cell takes four clock cycles in both in low and high frequency operational modes.

14. (Withdrawn) The DRR DRAM of claim 8, wherein:

said DDR DRAM is adapted to initiate, in a timed auto-precharge mode of low frequency operational mode, a precharge immediately after a falling edge of a clock cycle; and

said DDR DRAM is adapted to, in a non-timed auto-precharge mode of said test mode, to start an auto-precharge asynchronously after the falling edge of a clock cycle and after a timer allows enough time for a write-back to said DDR DRAM.

15. (Currently Amended) A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method, said method comprising the computer implemented steps of, in the order recited:

(a) placing a DDR DRAM having a test mode and an operational mode in test mode, said DDR RAM comprising an array of storage cells arranged in rows and columns, storage cells each row addressable by a respective wordline of a set of wordlines and each storage cells in each column addressable by a respective bitline of a set of bitlines;

(b) issuing a bank activate command on an occurrence of a rising edge of a first clock signal of a pair of adjacent clock signals of a test clock to select and bring up a wordline selected from said set of wordlines for write of said ~~DDR DRAM~~ wordline selected for write;

(c) ~~writing~~ issuing a write with auto-precharge [,] command on an occurrence of a rising edge of a second clock signal of said pair of adjacent clock signals to write a test pattern to storage cells ~~of said DDR DRAM~~ corresponding to said wordline selected for write;

(d) repeating steps (b) and (c) until all wordlines of said set of wordlines ~~for write~~ have been selected and written;

(e) issuing a bank activate command on an occurrence of a rising edge of a first clock signal of a subsequent pair of adjacent clock signals to select and bring up a wordline selected from said set of wordlines for read of said ~~DDR DRAM~~ wordline selected for read;

(f) ~~reading~~ issuing a read with auto-precharge [,] command on an occurrence of a rising edge of a second clock signal of said subsequent pair of adjacent clock signals to read the stored test pattern from storage cells ~~of said DDR DRAM~~ corresponding to said wordline selected for read; and

(g) repeating steps (e) and (f) until all wordlines of said set of wordlines ~~for read~~ have been selected and read.

16. (Currently Amended) The system of claim 15, wherein ~~each of steps (b), (c), (e) and (f) each take~~ a read column address select latency of said DDR DRAM is one clock cycle of said test clock.

17-18 (Canceled)

19. (Original) The system of claim 15, wherein said DDR DRAM is operating at a clock frequency below about one MHz in test mode.

20. (Original) The system of claim 15, wherein an amount of elapsed time between writing to and reading from a storage cell accessible by a particular wordline and bitline combination does not exceed a retention time specification of said storage cell.

21. (Currently Amended) The method of claim 1, further including:

(f h) comparing said test pattern to said stored test pattern.

22. (Currently Amended) The system of 15, the method further including:

(f h) comparing said test pattern to said stored test pattern.

23. (New) The method of claim 1, wherein step (c) further includes issuing a write burst enable command after said occurrence of said rising edge of said second clock signal of said pair of adjacent clock signals and completing said write burst enable command before a falling edge of said second clock signal of said pair of adjacent clock signals.

24. (New) The system of claim 15, wherein method step (c) further includes issuing a write burst enable command after said occurrence of said rising edge of said second clock signal of said pair of adjacent clock signals and completing said write burst enable command before an occurrence of a falling edge of said second clock signal of said pair of adjacent clock signals.

25. (New) The method of claim 1, wherein step (f) further includes issuing an auto-precharge reset command after an occurrence of a falling edge of said second clock signal of said subsequent pair of adjacent clock signals and completing said auto-precharge reset command before said occurrence of said rising edge of said first clock signal of said next pair of adjacent clock signals.

26. (New) The system of claim 15, wherein step (f) further includes issuing an auto-precharge reset command after an occurrence of a falling edge of said second clock signal of said subsequent pair of adjacent clock signals and completing said auto-precharge reset command before said occurrence of said rising edge of said first clock signal of said next pair of adjacent clock signals.

27. (New) The method of claim 1, wherein said write with auto-precharge command simultaneously issues a precharge command to precharge said set of bitlines to a known state and a write command to said wordline selected for write.

28. (New) The system of claim 15, wherein said write with auto-precharge command simultaneously issues a precharge command to precharge said set of bitlines to a known state and a write command to said wordline selected for write.

29. (New) The method of claim 1, wherein said read with auto-precharge command simultaneously issues a precharge command to precharge said set of bitlines to a known state and a read command to said wordline selected for read.

30. (New) The system of claim 15, wherein said read with auto-precharge command simultaneously issues a precharge command to precharge said set of bitlines to a known state and a write command to said wordline selected for read.